Programmable USB Type-C PD Controller

Hynetek Semiconductor Co., Ltd.

HUSB311

FEATURES

- Dual-Role PD Compatible
- Attach/Detach Detection as Host, Device or DRP
- Current Capability Definition and Detection
- Cable Recognition
- Dead Battery Support
- Ultra-low Power Mode for Attach Detection
- Simple I²C Interface with AP or EC
- BIST Mode Supported
- e-fuse IP
- 9-Ball WLCSP and 14-Lead QFN package

APPLICATIONS

- Smartphones
- Tablets
- Laptops

GENERAL DESCRIPTION

The HUSB311 is a USB Type-C controller that complies with the latest USB Type-C and PD standards. The HUSB311 integrates a complete Type-C Transceiver including the Rp and Rd resistors. It does the USB Type-C detection including attach and orientation. The HUSB311 integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

TYPICAL APPLICATION CIRCUIT

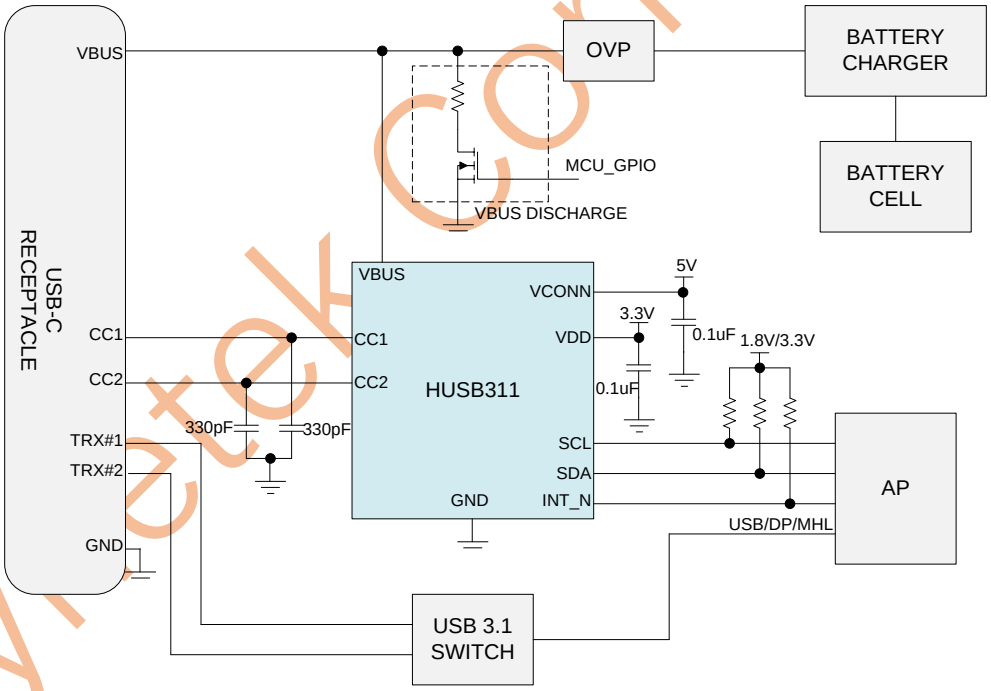


Figure 1. Typical Application Circuit

TABLE OF CONTENTS

REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	09/2020	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

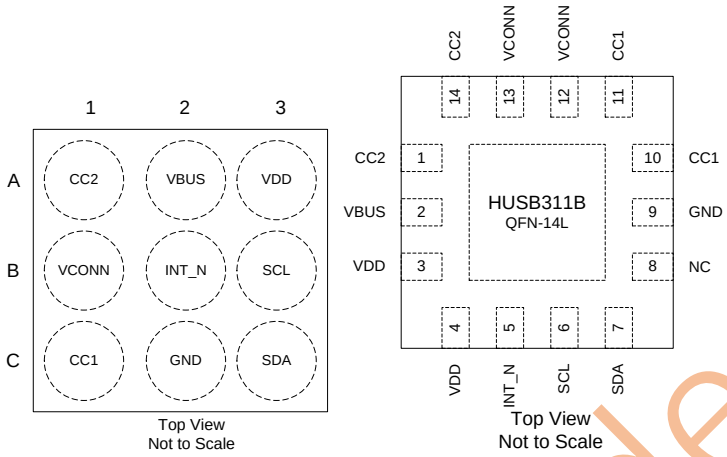


Figure 2. Pin Configuration (Top View)

Table 1. Pin Function Descriptions

HUSB311A Pin	HUSB311B Pin	NAME	Pin Type	Voltage Type	DESCRIPTION
A1	1, 14	CC2	A IO	HV	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
A2	2	VBUS	I	HV	VBUS input pin for attach and detach detection when operating as an UFP port (Device).
A3	3, 4	VDD	P	LV	Input supply voltage.
B1	12, 13	VCONN	P	LV	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories, and this pin must be powered up later 1ms than VDD.
B2	5	INT_N	OD	LV	Active low and open drain type interrupt output used to prompt the processor to read the registers.
B3	6	SCL	A IO	LV	I^2C serial clock signal to be connected to the I2C master. The address is 0x4E.
C1	10, 11	CC1	A IO	HV	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
C2	9	GND	P	-	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation and current flow.
C3	7	SDA	AD IO	LV	I^2C serial data signal to be connected to the I2C master. The address is 0x4E.
-	8	NC	-	-	Not connection

Legend:

HV=High Voltage Pin (Max 28V)

LV=Low Voltage Pin (Max 6V)

OD=Open Drain Pin

A=Analog Pin

P= Power Pin

D=Digital Pin

I=Input Pin

O=Output Pin

SPECIFICATIONS

V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GENERAL PARAMETERS						
Supply Voltage	V_{DD}		2.8	-	5.5	V
Supply UVLO voltage	$V_{IN\_UVLO\_RISE}$	Rising edge	-	2.7	-	V
	$V_{IN\_UVLO\_FALL}$	Falling edge	-	2.64	-	V
DRP Toggle Current consumption		VCONN power on	-	25	-	µA
		VCONN power off		20		µA
Supply Current at Normal Operation	I_{CC_OPR}	Idle mode	-	2.8	-	mA
CC1 & CC2 PINS						
Pull-down Voltage in Dead Battery	V_{DBL}	80uA±20%, VDD=0V	0.25		1.5	
	V_{DBH}	180uA±8%, VDD=0V	0.45		1.5	V
	V_{DBH}	330uA±8%, VDD=0V	0.85		2.45	V
Pull-down Resistor	R_D		4.6	5.1	5.6	kΩ
Voltage Threshold for Detecting a DFP at Default Mode	$V_{TH\_UFP\_DEF}$	Configured as a UFP	0.15	0.2	0.25	V
Voltage Threshold for Detecting a DFP at 1.5 A Mode	$V_{TH\_UFP\_1P5}$	Configured as a UFP	0.61	0.66	0.70	V
Voltage Threshold for Detecting a DFP at 3.0 A Mode	$V_{TH\_UFP\_3P0}$	Configured as a UFP	1.16	1.23	1.31	V
Voltage Threshold for Detecting a UFP at Default Mode	$V_{TH\_DFP\_DEF}$	Configured as a DFP	1.51	1.6	1.64	V
Voltage Threshold for Detecting a UFP at 1.5 A Mode	$V_{TH\_DFP\_1P5}$	Configured as a DFP	1.51	1.6	1.64	V
Voltage Threshold for Detecting a UFP at 3.0 A Mode	$V_{TH\_DFP\_3P0}$	Configured as a DFP	2.46	2.6	2.74	V
Ra Detection at Default Mode	$V_{TH\_RA\_DEF}$	Configured as a DFP	0.15	0.2	0.25	V
Ra Detection at 1.5 A Mode	$V_{TH\_RA\_1P5}$	Configured as a DFP	0.35	0.4	0.45	V
Ra Detection at 3.0 A Mode	$V_{TH\_RA\_3P0}$	Configured as a DFP	0.75	0.8	0.85	V
Default Mode Pullup Current Source	I_{CC_DEF}	Operate in DFP or DRP mode	64	80	96	µA
1.5 A Mode Pullup Current Source	I_{CC_1P5}	Operate in DFP or DRP mode	166	180	194	µA
3.0 A Mode Pullup Current Source	I_{CC_3P0}	Operate in DFP or DRP mode	304	330	356	µA
BMC BLOCK						
Bit Rate	fBitRate		270	300	330	Kbbs
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate.	pBitRate				0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble.	tInterFrameGap		25			µs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line.	tStartDrive		-1		1	µs
Time to cease driving the line after the end of the last bit of the Frame.	tEndDriveBMC				23	µs
Fall Time	tFall		300			ns

Time to cease driving the line after the final high-to-low transition.	tHoldLowBMC		1			µs
Rise Time	tRise		300			ns
Voltage Swing			1.050	1.125	1.200	V
TX Output Impedance	R_{TX}	PD TX mode	33	48	75	Ω
Time window for detecting non-idle	tTransitionWindow		12		20	µs
Receiver Input Impedance	zBmcRx		1			MΩ
VCONN PIN						
VCONN Power FET Resistance	R_{DS_ON}			0.75	1	Ω
VCONN OCP Threshold			500	650	800	mA
VCONN Present Threshold			2		2.4	V
VCONN Discharge Resistance		When VC_DISC_EN=1	4.6	5.1	5.6	kΩ
VCONN OVP Threshold			5.32	5.6	5.88	V
Time for VCONN to turn on				1.2		ms
VBUS PIN						
VBUS Present Threshold		Assert VBUS_PRESENT bit		3.8		V
VBUS Detection Valid Voltage				4		V
VBUS vSave0V		To trigger VBUS_80 flag		0.8		V
VBUS Measure Range			4	-	22	V
VBUS Measure Step		4V-10V range		0.5		V
		10V-20V range		1		V
VBUS_CONN Sense Threshold		Between 2'b0000 and 2'b0001	0.415	0.425	0.435	V
		Between 2'b0001 and 2'b0010	0.465	0.475	0.485	V
		Between 2'b0010 and 2'b0011	0.515	0.525	0.535	V
		Between 2'b0011 and 2'b0100	0.565	0.575	0.585	V
		Between 2'b0100 and 2'b0101	0.615	0.625	0.635	V
		Between 2'b0101 and 2'b0110	0.665	0.675	0.685	V
		Between 2'b0110 and 2'b0111	0.715	0.725	0.735	V
		Between 2'b0111 and 2'b1000	0.765	0.775	0.785	V
		Between 2'b1000 and 2'b1001	0.815	0.825	0.835	V
		Between 2'b1001 and 2'b1010	0.865	0.875	0.885	V
		Between 2'b1010 and 2'b1011	0.915	0.925	0.935	V
		Between 2'b1011 and 2'b1100	0.965	0.975	0.985	V
		Between 2'b1100 and 2'b1101	1.015	1.025	1.035	V
		Between 2'b1101 and 2'b1110	1.065	1.075	1.085	V
		Between 2'b1110 and 2'b1111	1.115	1.125	1.135	V
I^2C (SCL and SDA) PINS						
SCL Clock Frequency	f_{SCL}		1		1000	kHz
Supply Range	V_{DD_I2C}		1.5		3.6	V
Low Level Input Voltage	V_{IL}	Applies to SCL, SDA			0.4	V
High Level Input Voltage	V_{IH}	Applies to SCL, SDA	1.2			V
Low Level Output Voltage	V_{OL}	Applies to SDA			0.4	V
INT_N PIN						
Leakage Current			-1		1	µA
Low-level signal output voltage	V_{OL}				0.4	V
PROTECTIONS						
Thermal Shutdown Risng	t_{TSD_RISE}			130		°C
Thermal Shutdown Falling	t_{TSD_FALL}			110		°C

TSD debounce	t_{DB_TSD}		100	ms

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Value
VBUS	-0.3V to 30V
CC1, CC2 to GND	-0.3V to 24V
VDD, VCONN, INT_N, SDA, SCL to GND	-0.3V to 6V
Junction Temperature Range	-40°C -150°C
Storage Temperature Range	-65°C -150°C
VBUS/CC1/CC2 PIN ESD HBM (Human Body Model)	±2KV
VDD, VCONN, INT_N, SDA, SCL PIN ESD HBM (Human Body Model)	±2KV
ESD MM (Machine Model)	TBD V
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
WLCSP-9B	81.5	0.7	°C/W
QFN-14L	TBD	TBD	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FUNCTIONAL BLOCK DIAGRAM

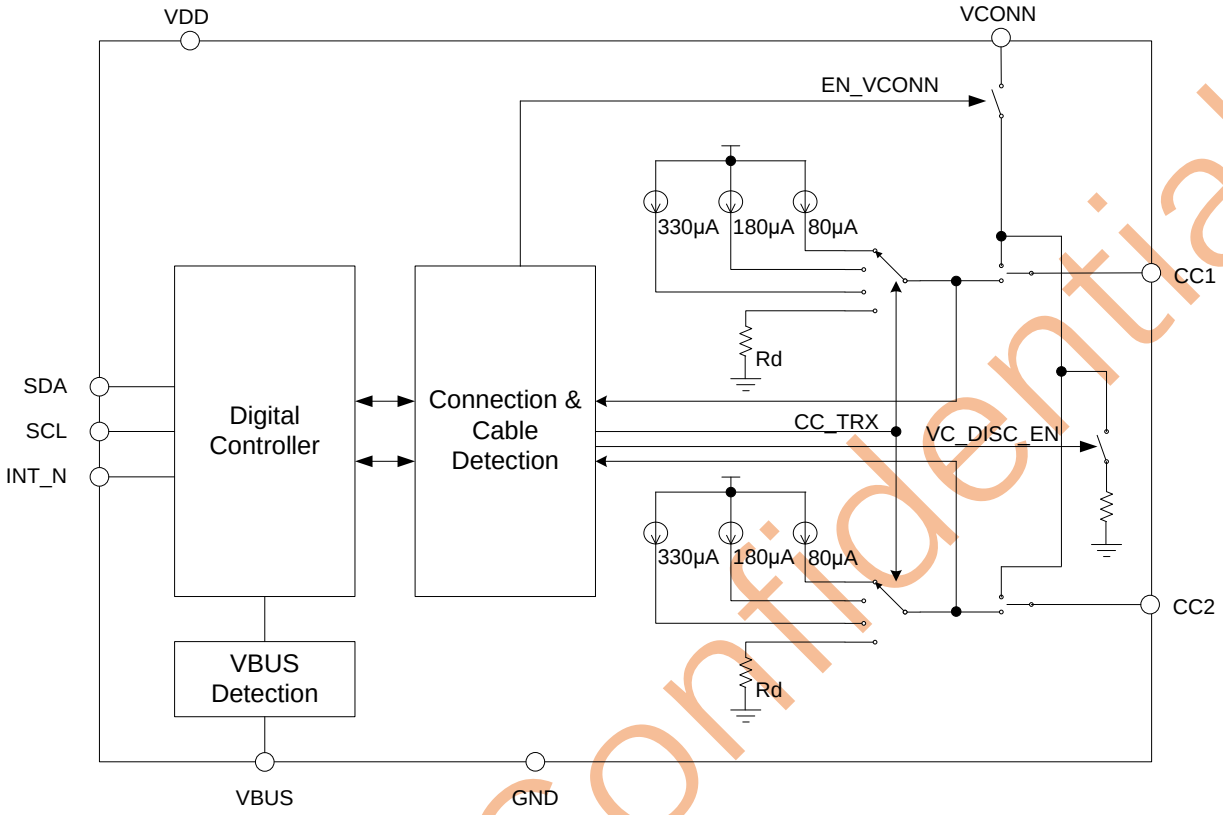


Figure 3. HUSB311 Functional Block Diagram

REGISTER MAP

HUSB311 has several registers to configure the functions. The registers are accessed by the I²C address of 0x4E. The detailed function is defined as below：

When there is register value change, the INT_N

Table 5. Legend of the Register Map

Tag	Name	Description
R	Read	This field may be read by I²C interface
W	Write	This field may be written by I²C interface
S	Set	This field may be set by a write of 1. Write of 0 has no effect.
C	Clear	This filed may be cleared by a write of 1. Write of 0 has no effect.
U	Update	This field is automatous update register.
L	Latch	This filed is latch register. A read clears the flag.

REGISTER MAP

All register is one bye length.

Add	Register Name	Bit	Bit Name	Def	Type	Description
0x00	VENDOR_ID	7:0	VID[7:0]	0x99	R	A unique 16-bit unsigned integer.
0x01		7:0	VID[15:8]	0x2E	R	Assigned by the USB-IF to the Vendor.
0x02	PRODUCT_ID	7:0	PID[7:0]	0x11	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03		7:0	PID[15:8]	0x03	R	
0x04	DEVICE_ID	7:0	DID[7:0]	0x00	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05		7:0	DID[15:8]	0x00	R	
0x06	USBTYPEC_REV	7:0	USBTYPEC_REV	0x11	R	Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001)
0x07		7:0	Reserved	0	R	
0x08	USBPD_REV_VER	7:0	USBPD_VER	0x11	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x09		7:0	USBPD_REV	0x20	R	0010 0000 – Revision 2.0
0x0A	PD_INTERFACE_REV	7:0	PDIF_VER	0x10	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x0B		7:0	PDIF_REV	0x10	R	0010 0000 – Revision 1.0
0x10	ALERT	7	ALARM_VBUS_VOLTAGE_H	0	R	Not support.
		6	TX_SUCCESS	0	RCU	0b: Cleared. 1b: Reset or SOP* message transmission successful.
		5	TX_DISCARD	0	RCU	0b: Cleared. 1b: Reset or SOP* message transmission not sent due to incoming receive message.
		4	TX_FAIL	0	RCU	0b: Cleared. 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
		3	RX_HARD_RESET	0	RCU	0b: Cleared. 1b: Received Hard Reset message.
		2	RX_SOP_MSG_STATUS	0	RCU	0b: Cleared, 1b: RECEIVE_BUFFER register changed. RX_BYTE_COUNT being set to 0 does not set this bit. The

Add	Register Name	Bit	Bit Name	Def	Type	Description
						RECEIVE_BUFFER comprises of three sets of registers: RX_BYTE_COUNT, RX_BUF_FRAME_TYPE and RX_BUF_BYTE_x (Register 0x30 to 0x4F).
		1	POWER_STATUS	0	RCU	0b: Cleared, 1b: Port status changed
		0	CC_STATUS	0	RCU	0b : Cleared, 1b : CC status changed
0x11	ALERT	7	Reserved	0	R	
		6	Reserved	0	R	
		5	Reserved	0	R	
		4	Reserved	0	R	
		3	Reserved	0	R	Not support.
		2	RXBUF_OVFLOW	0	RCU	0b: TCPC Rx buffer is functioning properly. 1b: TCPC Rx buffer has overflowed.
		1	FAULT	0	RCU	0b: No Fault. 1b: A Fault has occurred. Read the FAULT_STATUS register.
		0	Reserved	0	R	Not support.
0x12	ALERT_MASK	7	M_ALARM_VBUS_VOLTAGE_H	1	R	Not support
		6	M_TX_SUCCESS	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		5	M_TX_DISCARD	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked
		4	M_TX_FAIL	1	RW	0b: Interrupt masked. 1b : Interrupt unmasked.
		3	M_RX_HARD_RESET	1	RW	0b : Interrupt masked. 1b : Interrupt unmasked.
		2	M_RX_SOP_MSG_STATUS	1	RW	0b : Interrupt masked. 1b : Interrupt unmasked.
		1	M_POWER_STATUS	1	RW	0b : Interrupt masked. 1b : Interrupt unmasked.
		0	M_CC_STATUS	1	RW	0b : Interrupt masked. 1b : Interrupt unmasked.
0x13	ALERT_MASK	7	Reserved	0	R	
		6	Reserved	0	R	
		5	Reserved	0	R	
		4	Reserved	0	R	
		3	Reserved	1	R	Not support.
		2	M_RXBUF_ OVFLOW	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		1	M_FAULT	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		0	M_ALARM_VBUS_VOLTAGE_L	1	R	Not support.
0x14	POWER_STATUS_MASK	7	Reserved	0	R	Not support.
		6	M_TCPC_INITIAL	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		5	M_SRC_HV	1	R	Not support.
		4	M_SRC_VBUS	1	R	Not support.

Add	Register Name	Bit	Bit Name	Def	Type	Description
		3	M_VBUS_PRESENT_DETC	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		2	M_VBUS_PRESENT	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		1	M_VCONN_ PRESENT	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		0	M_SINK_VBUS	1	R	Not support.
0x15	FAULT_STATUS_MASK	7	M_VCON_OV	0	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		6	M_FORCE_OFF_VBUS	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
		5	M_AUTO_DISC_FAIL	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
		4	M_FORCE_DISC_FAIL	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
		3	M_VBUS_OC	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
		2	M_VBUS_OV	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
		1	M_VCON_OC	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked.
		0	M_I2C_ERROR	1	RW	0b: Interrupt masked. 1b: Interrupt unmasked. This field has no meaning for HUSB311.
0x18	CONFIG_STANDARD_OUTPUT	7	H_IMPEDENCE	0	R	Not support.
		6	DBG_ACC_CONNECT_O	0	R	Not support.
		5	AUDIO_ACC_CONNECT	0	R	Not support.
		4	ACTIVE_CABLE_CONNECT	0	R	Not support.
		3:2	MUX_CTRL	0	R	Not support.
		1	CONNECT_PRESENT	0	R	Not support.
		0	CONNECT_ORIENT	0	R	Not support.
0x19	TCPC_CONTROL	7:5	Reserved	0	R	
		4	Reserved	0	R	
		3:2	I2C_CK_STRETCH	00	R	Not support.
		1	BIST_TEST_MODE	0	RW	0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.

Add	Register Name	Bit	Bit Name	Def	Type	Description
		0	PLUG_ORIENT	0	RW	0b: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.
0x1A	ROLE_CONTROL	7	Reserved	0	R	
		6	DRP	0	RW	0b: No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
		5:4	RP_VALUE	0	RW	00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved
		3:2	CC2	10	RW	00b : Reserved 01b: Rp (Use Rp definition in B5..4) 10b : Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
		1:0	CC1	10	RW	00b : Reserved 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
0x1B	FAULT_CONTROL	7	DIS_VCON_OV	0	RW	0b: Fault detection circuit enabled. 1b: Fault detection circuit disabled.
		6:5	Reserved	0	R	
		4	DIS_FORCE_OFF_VBUS	0	R	Not support.
		3	DIS_VBUS_DISC_FAULT_TIMER	0	R	Not support.
		2	DIS_VBUS_OC	0	R	Not support.
		1	DIS_VBUS_OV	0	R	Not support.
		0	DIS_VCON_OC	0	RW	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled
0x1C	POWER_CONTROL	7	Reserved	0	R	
		6	VBUS_VOL_ MONITOR	0	R	Not support.
		5	DIS_VOL_ALARM	0	R	Not support.
		4	AUTO_DISC_ DISCNCT	0	R	Not support.
		3	BLEED_DISC	0	R	Not support.
		2	FORCE_DISC	0	R	Not support.
		1	VCONN_ POWER_SPT	0	RW	0b: TCPC delivers at least 1W on VCONN. 1b: TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONN_POWER.
		0	EN_VCONN	0	RW	0b: Disable VCONN Source (default). 1b: Enable VCONN Source to CC Required.
0x1D	CC_STATUS	7:6	Reserved	0	R	
		5	DRP_STATUS	0	RU	0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00). 1b: the TCPC is toggling.
		4	DRP_RESULT	0	RU	0b: the TCPC is presenting Rp. 1b: the TCPC is presenting Rd.

Add	Register Name	Bit	Bit Name	Def	Type	Description

		3:2	CC2_STATUS	00	RU	If (ROLE_CONTROL.CC2 = Rp) or (DRP_RESULT = 0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC2 = Rd) or (DRP_RESULT = 1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
						
						~~If ROLE_CONTROL.CC2 = Ra, this field is set to 00b~~
						If ROLE_CONTROL.CC2 = Open, this field is set to 00b
						
						This field always returns 00b if (DRP_STATUS = 1) or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT =0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

0x1D	CC_STATUS	1:0	CC1_STATUS	0	RU	If (ROLE_CONTROL.CC1 = Rp) or (DrpResult = 0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC1 = Rd) or DrpResult = 1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
						
						~~If ROLE_CONTROL.CC1 = Ra, this field is set to 00b~~
						If ROLE_CONTROL.CC1 = Open, this field is set to 00b
						
						This field always returns 00b if (DRP_STATUS = 1) or (POWER_CONTROL.EN_VCONN = 1 and TCPC_CONTROL.PLUG_ORIENT = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

0x1E	POWER_STATUS	7	DBG_ACC_CONNECT	0	R	Not support.
		6	TCPC_INITIAL	0	RU	0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh
		5	SRC_HV	0	R	Not support.
		4	SRC_VBUS	0	R	Not support.
		3	VBUS_PRESENT_DETC	1	RU	0b: VBUS Present Detection Disabled. 1b: VBUS Present Detection Enabled (default).
		2	VBUS_PRESENT	0	RU	0b: VBUS Disconnected. 1b: VBUS Connected.

Add	Register Name	Bit	Bit Name	Def	Type	Description
		1	VCONN_PRESENT	0	RU	0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V When Ra is detected and IC enter attached.SRC, VCONN is enabled.
		0	SINK_VBUS	0	R	Not support.
0x1F	FAULT_STATUS	7	VCON_OV	0	RCU	0b: Not in an over-voltage protection state 1b: Over-voltage fault latched.
		6	FORCE_OFF_VBUS	0	R	Not support.
		5	AUTO_DISC_FAIL	0	R	Not support.
		4	FORCE_DISC_FAIL	0	R	Not support.
		3	VBUS_OC	0	R	Not support.
		2	VBUS_OV	0	R	Not support.
		1	VCON_OC	0	RCU	0b: No Fault detected. 1b: Over-current VCONN fault latched.
		0	I2C_ERROR	0	RCU	0b: No Error. 1b: I2C error has occurred. A TRANSMIT has been sent with an empty TRANSMIT_BUFFER. This field has no meaning for HUSB311.
0x20		7:0	Reserved	0	R	
0x21		7:0	Reserved	0	R	
0x22		7:0	Reserved	0	R	
0x23	COMMAND	7:0	COMMAND	0	R	Write 0x99 for Look4Connection.
0x24	DEVICE_CAPABILITIES_1L	7:5	ROLES_SUPPORT	110	R	000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP). 001b: Source only. 010b: Sink only. 011b: Sink with accessory support (optional). 100b: DRP only. ~~101b: Adapter or Cable (Ra) only~~ 110b: Source, Sink, DRP, Adapter/Cable all supported. 111b: Not valid.
		4	ALL_SOP_SUPPORT	1	R	0b: All SOP* except SOP'_DBG/SOP"_DBG. 1b: All SOP* messages are supported.
		3	SOURCE_VCONN	1	R	0b: TCPC is not capable of switching VCONN. 1b: TCPC is capable of switching VCONN.
		2	CPB_SINK_VBUS	0	R	0b: TCPC is not capable controlling the sink path to the system load. 1b: TCPC is capable of controlling the sink path to the system load.
		1	SOURCE_HV_VBUS	0	R	0b: TCPC is not capable of controlling the source high voltage path to VBUS. 1b: TCPC is capable of controlling the source high voltage path to VBUS.
		0	SOURCE_VBUS	0	R	0b: TCPC is not capable of controlling the source path to VBUS. 1b: TCPC is capable of controlling the source path to VBUS.
0x25	DEVICE_CAPABILITIES_1H	7	Reserved	0	R	

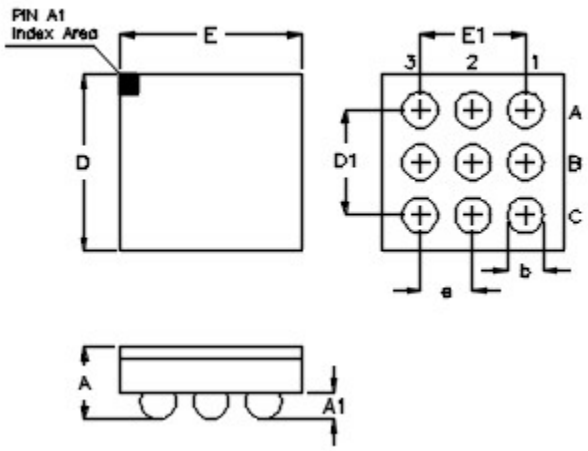
Add	Register Name	Bit	Bit Name	Def	Type	Description
		6	CPB_VBUS_OC	0	R	0b: VBUS OCP is not reported by the TCPC. 1b: VBUS OCP is reported by the TCPC.
		5	CPB_VBUS_OV	0	R	0b: VBUS OVP is not reported by the TCPC. 1b: VBUS OVP is reported by the TCPC.
		4	CPB_BLEED_DISC	0	R	0b: No Bleed Discharge implemented in TCPC. 1b: Bleed Discharge is implemented in the TCPC.
		3	CPB_FORCE_DISC	0	R	0b: No Force Discharge implemented in TCPC. 1b: Force Discharge is implemented in the TCPC.
		2	VBUS_MEASURE_ALARM	0	R	0b: No VBUS voltage measurement nor VBUS Alarms. 1b: VBUS voltage measurement and VBUS Alarms.
		1:0	SOURCE_RP_SUPPORT	10	R	00b: Rp default only. 01b: Rp 1.5A and default. 10b: Rp 3.0A, 1.5A, and default. 11b: Reserved. Rp values which may be configured by the TCPM via the ROLE_CONTROL register.
0x26	DEVICE_CAPABILITIES_2L	7	SINK_DISCONNECT_DET	0	R	0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VBUS_PRESENT=0b to indicate a Sink disconnect). 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented.
		6	STOP_DISC_THD	0	R	0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented.
		5:4	VBUS_VOL_ALARM_LSB	11	R	00: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: reserved
		3:1	VCONN_POWER	010	R	000b: 1.0W. 001b: 1.5W. 010b: 2.0W. 011b: 3W. 100b: 4W. 101b: 5W. 110b: 6W. 111b: External.
		0	VCONN_OCF	1	R	0b: TCPC is not capable of detecting a VCONN over-current fault. 1b: TCPC is capable of detecting a VCONN over-current fault.
0x27	DEVICE_CAPABILITIES_2H	7:0	Reserved	0	R	
0x28		7:3	Reserved	0	R	

Add	Register Name	Bit	Bit Name	Def	Type	Description
	STANDARD_INPUT_CAPABILITIES	2	VBUS_EXT_OVF	0	R	Not support.
		1	VBUS_EXT_OCF	0	R	Not support.
		0	FORCE_OFF_ VBUS_IN	0	R	Not support.
0x29	STANDARD_OUTPUT_CAPABILITIES	7	Reserved	0	R	
		6	CPB_DBG_ ACC_IND	0	R	Not support.
		5	CPB_VBUS_PRESENT_MNT	0	R	Not support.
		4	CPB_AUDIO_ADT_ACC_IND	0	R	Not support.
		3	CPB_ACTIVE_CABLE_IND	0	R	Not support.
		2	CPB_MUX_CFG_CTRL	0	R	Not support.
		1	CPB_CONNECT_PRESENT	0	R	Not support.
		0	CPB_CONNECT_ORIENT	0	R	Not support.
0x2E	MESSAGE_HEADER_INFO	7:5	Reserved	0	R	
		4	CABLE_PLUG	0	RW	0b: Message originated from Source, Sink, or DRP, 1b: Message originated from a Cable Plug,
		3	DATA_ROLE	0	RW	0b: UFP 1b: DFP
		2:1	USBPD_SPECREV	01	RW	00b: Revision 1.0. 01b: Revision 2.0. 10b – 11b: Reserved,
		0	POWER_ROLE	0	RW	0b: Sink. 1b: Source.
0x2F	RECEIVE_DETECT	7	Reserved	0	R	
		6	EN_CABLE_RST	0	RWU	0b : TCPC does not detect Cable Reset signaling (default) 1b : TCPC detects Cable Reset signaling
		5	EN_HARD_RST	0	RWU	0b: TCPC does not detect Hard Reset signaling (default) 1b : TCPC detects Hard Reset signaling
		4	EN_SOP2DB	0	RWU	0b: TCPC does not detect SOP_DBG'' message (default) 1b : TCPC detects SOP_DBG'' message
		3	EN_SOP1DB	0	RWU	0b : TCPC does not detect SOP_DBG' message (default) 1b : TCPC detects SOP_DBG' message
		2	EN_SOP2	0	RWU	0b : TCPC does not detect SOP'' message (default) 1b : TCPC detects SOP'' message
		1	EN_SOP1	0	RWU	0b : TCPC does not detect SOP' message (default) 1b : TCPC detects SOP' message
		0	EN_SOP	0	RWU	0b : TCPC does not detect SOP message (default) 1b : TCPC detects SOP message
0x30	RX_BYTE_COUNT	7:0	RX_BYTE_COUNT	0	RU	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	RX_BUF_FRAME_TYPE	7:3	Reserved	0	R	
		2:0	RX_FRAME_TYPE	0	RU	Type of received frame 000b : Received SOP 001b : Received SOP' 010b : Received SOP'' 011b : Received SOP_DBG' 100b : Received SOP_DBG'' 110b : Received Cable Reset All others are reserved.

Add	Register Name	Bit	Bit Name	Def	Type	Description
0x32	RX_BUF_HEADER_BYTE_0	7:0	RX_HEAD_0	0	RU	Byte 0 (bits 7..0) of message header
0x33	RX_BUF_HEADER_BYTE_1	7:0	RX_HEAD_1	0	RU	Byte 1 (bits 15..8) of message header
0x34	RX_BUF_OBJ1_BYTE_0	7:0	RX_OBJ1_0	0	R	Byte 0 (bits 7..0) of 1st data object
0x35	RX_BUF_OBJ1_BYTE_1	7:0	RX_OBJ1_1	0	R	Byte 1 (bits 15..8) of 1st data object
0x36	RX_BUF_OBJ1_BYTE_2	7:0	RX_OBJ1_2	0	R	Byte 2 (bits 23..16) of 1st data object
0x37	RX_BUF_OBJ1_BYTE_3	7:0	RX_OBJ1_3	0	R	Byte 3 (bits 31..24) of 1st data object
0x38	RX_BUF_OBJ2_BYTE_0	7:0	RX_OBJ2_0	0	R	Byte 0 (bits 7..0) of 2nd data object
0x39	RX_BUF_OBJ2_BYTE_1	7:0	RX_OBJ2_1	0	R	Byte 1 (bits 15..8) of 2nd data object
0x3A	RX_BUF_OBJ2_BYTE_2	7:0	RX_OBJ2_2	0	R	Byte 2 (bits 23..16) of 2nd data object
0x3B	RX_BUF_OBJ2_BYTE_3	7:0	RX_OBJ2_3	0	R	Byte 3 (bits 31..24) of 2nd data object
0x3C	RX_BUF_OBJ3_BYTE_0	7:0	RX_OBJ3_0	0	R	Byte 0 (bits 7..0) of 3rd data object
0x3D	RX_BUF_OBJ3_BYTE_1	7:0	RX_OBJ3_1	0	R	Byte 1 (bits 15..8) of 3rd data object
0x3E	RX_BUF_OBJ3_BYTE_2	7:0	RX_OBJ3_2	0	R	Byte 2 (bits 23..16) of 3rd data object
0x3F	RX_BUF_OBJ3_BYTE_3	7:0	RX_OBJ3_3	0	R	Byte 3 (bits 31..24) of 3st data object
0x40	RX_BUF_OBJ4_BYTE_0	7:0	RX_OBJ4_0	0	R	Byte 0 (bits 7..0) of 4th data object
0x41	RX_BUF_OBJ4_BYTE_1	7:0	RX_OBJ4_1	0	R	Byte 1 (bits 15..8) of 4th data object
0x42	RX_BUF_OBJ4_BYTE_2	7:0	RX_OBJ4_2	0	R	Byte 2 (bits 23..16) of 4th data object
0x43	RX_BUF_OBJ4_BYTE_3	7:0	RX_OBJ4_3	0	R	Byte 3 (bits 31..24) of 4th data object
0x44	RX_BUF_OBJ5_BYTE_0	7:0	RX_OBJ5_0	0	R	Byte 0 (bits 7..0) of 5th data object
0x45	RX_BUF_OBJ5_BYTE_1	7:0	RX_OBJ5_1	0	R	Byte 1 (bits 15..8) of 5th data object
0x46	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0	R	Byte 2 (bits 23..16) of 5th data object
0x47	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0	R	Byte 3 (bits 31..24) of 5th data object
0x48	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0	R	Byte 0 (bits 7..0) of 6th data object
0x49	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0	R	Byte 1 (bits 15..8) of 6th data object
0x4A	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0	R	Byte 2 (bits 23..16) of 6th data object
0x4B	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0	R	Byte 3 (bits 31..24) of 6st data object
0x4C	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0	R	Byte 0 (bits 7..0) of 7th data object
0x4D	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0	R	Byte 1 (bits 15..8) of 7th data object
0x4E	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0	R	Byte 2 (bits 23..16) of 7th data object
0x4F	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0	R	Byte 3 (bits 31..24) of 7th data object
0x50	TX_BUF_FRAME_TYPE	7:6	Reserved	0	R	
		5:4	TX_RETRY_ CNT	0	RWU	00b: No message retry is required. 01b: Automatically retry message transmission once. 10b: Automatically retry message transmission twice. 11b: Automatically retry message transmission three times.
		3	Reserved	0	R	
		2:0	TX_FRAME_ TYPE	0	RWU	000b: Transmit SOP. 001b: Transmit SOP'. 010b: Transmit SOP". 011b: Transmit SOP_DBG'. 100b: Transmit SOP_DBG". 101b: Transmit Hard Reset. 110b: Transmit Cable Reset. 111b: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max).

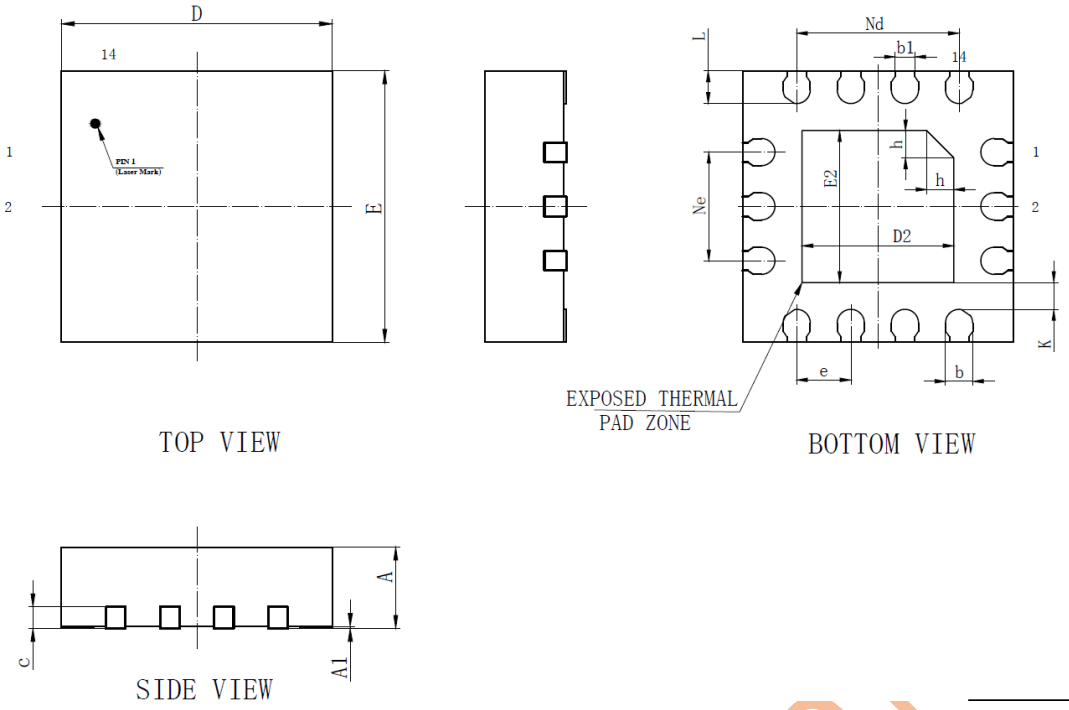
Add	Register Name	Bit	Bit Name	Def	Type	Description
0x51	TX_BYTE_COUNT	7:0	TX_BYTE_ COUNT	0	RWU	The number of bytes the TCPM will write
0x52	TX_BUF_HEADER_BYTE_0	7:0	TX_HEAD_0	0	RWU	Byte 0 (bits 7..0) of message header
0x53	TX_BUF_HEADER_BYTE_1	7:0	TX_HEAD_1	0	RW	Byte 1 (bits 15..8) of message header
0x54	TX_BUF_OBJ1_BYTE_0	7:0	TX_OBJ1_0	0	RW	Byte 0 (bits 7..0) of 1st data object
0x55	TX_BUF_OBJ1_BYTE_1	7:0	TX_OBJ1_1	0	RW	Byte 1 (bits 15..8) of 1st data object
0x56	TX_BUF_OBJ1_BYTE_2	7:0	TX_OBJ1_2	0	RW	Byte 2 (bits 23..16) of 1st data object
0x57	TX_BUF_OBJ1_BYTE_3	7:0	TX_OBJ1_3	0	RW	Byte 3 (bits 31..24) of 1st data object
0x58	TX_BUF_OBJ2_BYTE_0	7:0	TX_OBJ2_0	0	RW	Byte 0 (bits 7..0) of 2nd data object
0x59	TX_BUF_OBJ2_BYTE_1	7:0	TX_OBJ2_1	0	RW	Byte 1 (bits 15..8) of 2nd data object
0x5A	TX_BUF_OBJ2_BYTE_2	7:0	TX_OBJ2_2	0	RW	Byte 2 (bits 23..16) of 2nd data object
0x5B	TX_BUF_OBJ2_BYTE_3	7:0	TX_OBJ2_3	0	RW	Byte 3 (bits 31..24) of 2nd data object
0x5C	TX_BUF_OBJ3_BYTE_0	7:0	TX_OBJ3_0	0	RW	Byte 0 (bits 7..0) of 3rd data object
0x5D	TX_BUF_OBJ3_BYTE_1	7:0	TX_OBJ3_1	0	RW	Byte 1 (bits 15..8) of 3rd data object
0x5E	TX_BUF_OBJ3_BYTE_2	7:0	TX_OBJ3_2	0	RW	Byte 2 (bits 23..16) of 3rd data object
0x5F	TX_BUF_OBJ3_BYTE_3	7:0	TX_OBJ3_3	0	RW	Byte 3 (bits 31..24) of 3rd data object
0x60	TX_BUF_OBJ4_BYTE_0	7:0	TX_OBJ4_0	0	RW	Byte 0 (bits 7..0) of 4th data object
0x61	TX_BUF_OBJ4_BYTE_1	7:0	TX_OBJ4_1	0	RW	Byte 1 (bits 15..8) of 4th data object
0x62	TX_BUF_OBJ4_BYTE_2	7:0	TX_OBJ4_2	0	RW	Byte 2 (bits 23..16) of 4th data object
0x63	TX_BUF_OBJ4_BYTE_3	7:0	TX_OBJ4_3	0	RW	Byte 3 (bits 31..24) of 4th data object
0x64	TX_BUF_OBJ5_BYTE_0	7:0	TX_OBJ5_0	0	RW	Byte 0 (bits 7..0) of 5th data object
0x65	TX_BUF_OBJ5_BYTE_1	7:0	TX_OBJ5_1	0	RW	Byte 1 (bits 15..8) of 5th data object
0x66	TX_BUF_OBJ5_BYTE_2	7:0	TX_OBJ5_2	0	RW	Byte 2 (bits 23..16) of 5th data object
0x67	TX_BUF_OBJ5_BYTE_3	7:0	TX_OBJ5_3	0	RW	Byte 3 (bits 31..24) of 5th data object
0x68	TX_BUF_OBJ6_BYTE_0	7:0	TX_OBJ6_0	0	RW	Byte 0 (bits 7..0) of 6th data object
0x69	TX_BUF_OBJ6_BYTE_1	7:0	TX_OBJ6_1	0	RW	Byte 1 (bits 15..8) of 6th data object
0x6A	TX_BUF_OBJ6_BYTE_2	7:0	TX_OBJ6_2	0	RW	Byte 2 (bits 23..16) of 6th data object
0x6B	TX_BUF_OBJ6_BYTE_3	7:0	TX_OBJ6_3	0	RW	Byte 3 (bits 31..24) of 6th data object
0x6C	TX_BUF_OBJ7_BYTE_0	7:0	TX_OBJ7_0	0	RW	Byte 0 (bits 7..0) of 7th data object
0x6D	TX_BUF_OBJ7_BYTE_1	7:0	TX_OBJ7_1	0	RW	Byte 1 (bits 15..8) of 7th data object
0x6E	TX_BUF_OBJ7_BYTE_2	7:0	TX_OBJ7_2	0	RW	Byte 2 (bits 23..16) of 7th data object
0x6F	TX_BUF_OBJ7_BYTE_3	7:0	TX_OBJ7_3	0	RW	Byte 3 (bits 31..24) of 7th data object

PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.300	1.380	0.051	0.054
D1	0.800		0.031	
E	1.340	1.420	0.053	0.056
E1	0.800		0.031	
e	0.400		0.016	

Figure 4. WLCSP-9B Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.20REF		
D	2.40	2.50	2.60
D2	1.30	1.40	1.50
e	0.50BSC		
Ne	1.00BSC		
Nd	1.50BSC		
E	2.40	2.50	2.60
E2	1.30	1.40	1.50
L	0.25	0.30	0.35
h	0.20	0.25	0.30
K	0.25REF		

Figure 5. QFN-14L Package

ORDERING GUIDE

IMPORTANT NOTICE

Hynetek Semiconductor Co., Ltd. and its subsidiaries (Hynetek) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to Hynetek’s terms and conditions of sale supplied at the time of order acknowledgment.

Hynetek warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in Hynetek’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent Hynetek deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

Hynetek assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using Hynetek components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Hynetek does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which Hynetek components or services are used. Information published by Hynetek regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Hynetek under the patents or other intellectual property of Hynetek.

Reproduction of significant portions of Hynetek information in Hynetek data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Hynetek is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of Hynetek components or services with statements different from or beyond the parameters stated by Hynetek for that component or service voids all express and any implied warranties for the associated Hynetek component or service and is an unfair and deceptive business practice.

Hynetek is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Hynetek components in its applications, notwithstanding any applications-related information or support that may be provided by Hynetek. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify Hynetek and its representatives against any damages arising out of the use of any Hynetek components in safety-critical applications.

In some cases, Hynetek components may be promoted specifically to facilitate safety-related applications. With such components, Hynetek’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No Hynetek components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those Hynetek components which Hynetek has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of Hynetek components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Hynetek has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, Hynetek will not be responsible for any failure to meet ISO/TS16949.

Please refer to below URL for other products and solutions of Hynetek Semiconductor Co., Ltd.